WHAT IS CLAIMED IS:

1. A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting an overlapped portion where a line portion overlaps a contact portion;

extracting a space width between the overlapped portion and another line portion adjoining the overlapped portion, and a line width of the line portion;

obtaining a variation curve representing a relationship between the space width and an amount of variation of the line width which occurs after a wafer process;

dividing the variation curve per design grid width and extracting intersections between the design grid width and the variation curve;

dividing the variation curve for intersection parts and establishing a correction rule for correcting integer times the design grid width with respect to each of the intersection parts; and

obtaining a relationship between the space width and the correction rule and correcting the overlapped portion based on the correction rule corresponding to the obtained relationship.

2. A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting an overlapped portion where a line

portion overlaps a contact portion;

extracting a space width between the overlapped portion and another line portion adjoining this overlapped portion, and a line width of the line portion;

obtaining a variation curve representing a relationship between the space width and an amount of a shortening of the line portion which occurs after wafer process;

dividing the variation curve per design grid width and extracting intersections between the design grid width and the variation curve;

dividing the variation curve for intersection parts and establishing a correction rule for correcting integer times the design grid width with respect to each of the intersection parts; and

obtaining a relationship between the space width and the correction rule and correcting the overlapped portion based on the correction rule corresponding to the obtained relationship.

3. A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting an overlapped portion where a line portion overlaps a contact portion;

enlarging the contact portion;

extracting a side where the enlarged portion is in contact with the end of the line portion;

extracting the space width between the side in contact and another line portion adjoining the side in contact, and the line width of the line portion;

obtaining a variation curve representing a relationship between the space width and an amount of a shortening of the line portion which occurs after wafer process;

dividing the variation curve per design grid width and extracting intersections between the design grid width and the variation curve;

dividing the variation curve for intersection parts and establishing a correction rule for correcting integer times the design grid width with respect to each of the intersection parts; and

obtaining a relationship between the space width and the correction rule and correcting the overlapped portion based on the correction rule corresponding to the obtained relationship.

4. A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting a gate end portion which is located not on a transistor portion but in the end of a line portion;

extracting an area of the gate end portion;

obtaining a variation curve representing a relationship between the area and an amount of shortening of the line portion which occur after wafer

process;

dividing the variation curve per design grid width and extracting intersections between the design grid width and the variation curve;

dividing the variation curve for intersection parts and establishing a correction rule for correcting integer times the design grid width with respect to each of the intersection parts; and

obtaining a relationship between the space width and the correction rule and correcting the gate end portion based on the correction rule corresponding to the obtained relationship.

5. A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting a corner portion of a transistor portion;

extracting the distance from the corner portion to a line portion;

obtaining the distance where the line portion does not overlap rounding of the corner portion generated after wafer process;

making a correction rule for a correction whether the corner portion is notched or not from the obtained distance; and

obtaining the corresponding relationship between the distance and the intersection part and making a correction based on the correction rule to the corner

portion.

6. A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting a first portion where a transistor option overlaps a contact portion and a second portion where a gate overlaps the contact portion;

extracting the diameter of the first portion and the diameter of the second distemper;

obtaining the relationship between the design dimension of the contact portion and the difference between the diameter of the first portion generated after wafer process and the diameter of the second portion;

dividing the obtained relationship per design grid width and extracting an intersection between this design grid width and the obtained relationship;

dividing the obtained relationship per intersection part and establishing a correction rule for correcting integer times of the design grid width per intersection part; and

obtaining the corresponding relationship between the design dimension and the intersection part and making a correction based on the correction rule to the first portion and the second portion.

7. A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting a portion where a line portion overlaps

a contact portion;

extracting the space width between the overlapped portion and another line potion adjoining this overlapped portion, the line width of the line portion, and the distance from the above contact portion to the end of the line portion;

obtaining the relationship between the space width and a shortening amount of the line portion generated after wafer process;

dividing the obtained relationship per design grid width and extracting an intersection between this design grid width and the obtained relationship;

dividing the obtained relationship per intersection part and establishing a correction rule for correcting integer times of the design grid width per intersection part; and

obtaining the corresponding relationship between the space width and the intersection part and making a correction based on the correction rule to the overlapped portion with the extracted distance as reference.

8. The pattern correcting method of a mask for manufacturing a semiconductor device according to claim 1, wherein the correction rule includes alignment margin.

9. The pattern correcting method of a mask for manufacturing a semiconductor device according to

claim 2, wherein the correction rule includes alignment margin.

10. The pattern correcting method of a mask for manufacturing a semiconductor device according to claim 3, wherein the correction rule includes alignment margin.

11. The pattern correcting method of a mask for manufacturing a semiconductor device according to claim 4, wherein the correction rule includes alignment margin.

12. The pattern correcting method of a mask for manufacturing a semiconductor device according to claim 5, wherein the correction rule includes alignment margin.

13. The pattern correcting method of a mask for manufacturing a semiconductor device according to claim 7, wherein the correction rule includes alignment margin.

14. A pattern correcting method of a mask for manufacturing a semiconductor device comprising:

extracting a portion where a contact portion overlaps a transistor portion;

extracting the space width to another transistor portion adjoining the transistor portion, and the distance from the transistor portion end to the overlapped portion;

enlarging the contact portion by the minimum

fringe amount prescribed by a design rule;

obtaining the relationship between the space width and a correction value for correcting the end of the transistor portion according to the space width;

dividing the obtained relationship per design grid width and extracting an intersection between this design grid width and the obtained relationship;

dividing the obtained relationship per intersection part and establishing a correction rule for correcting integer times of the design grid width per intersection part; and

obtaining the corresponding relationship between the space width and the intersection part and making a correction based on the correction rule to the end of the transistor portion, wherein

the correction is made to the entire end of the transistor portion when the distance from the transistor portion end to the overlapped portion is larger than the minimum fringe amount and to the end of the transistor portion except the part where the enlarged contact portion is in contact when the distance from the transistor portion end to the overlapped portion is less than the minimum fringe amount.

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